501.43126X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: H. OGASAWARA, et al

Serial No.: 10/673,162

Filing Date: September 30, 2003

Title: STORAGE DEVICE SYSTEM AND STORAGE DEVICE SYSTEM ACTIVATING METHOD

Art Unit: 2171

PETITION TO MAKE SPECIAL
UNDER 37 CFR 1.102(d) and MPEP. §708.02, VIII

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 17, 2004

Sir:

1. Petition

Applicants hereby petition to make this application **Special**, in accordance with 37 CFR §1.102(d) and MPEP 708.02, VIII. The present invention is a new application filed in the United States Patent and Trademark Office September 30, 2003 and as such has not received any examination by the Examiner.

2. Claims

Applicants hereby represent that all the claims in the present application are directed to a single invention. If upon examination it is the Office determined that all the claims presented are not directed to a single invention, Applicants will make an election without traverse as a prerequisite to the grant of special status.

3. Search

Applicants hereby submit that a pre-examination search has been made by a professional searcher in the following classes and subclasses:

Class	Subclass
709	217, 219, 224, 225
711	112, 113, 118, 147, 148, 150, 161, 162
714	6

4. Copy of References

A listing of all references found by the professional searcher is provided by a Form PTO-1449 and copies of the references and the Form PTO-1449 are submitted as part of an Information Disclosure Statement (IDS) filed on even date.

5. Detailed Discussion of the References and Distinctions Between the References and the Claims

Below is a detailed discussion of three references cited in the IDS filed on even date that appear to be most closely related to the subject matter encompassed by the claims of the present application, and which discussion particularly points out how Applicants' claimed subject matter is distinguishable over those references. All other references cited in the IDS filed on closely related to the subject matter encompassed by the claims of the present application are **not** treated in detail herein.

a. Detailed Discussion of the References

U.S. Patent No. 5,928,327 (Wang et al) discloses a system which includes one or more central control modules (CCM)'s, one or more delivery modules (DM)'s and one or more storage modules (SM)'s. Each CCM is a conventional computer equipped with two conventional Small Computer Serial Interface (SCSI) cards, each operating in an "initiator" mode for interfacing with one or more DM's and SM's

respectively. Each CCM also has local memory used as an intermediate memory buffer to store data retrieved from a SM prior to delivery to a DM. Each CCM additionally has a communication interface for coupling to a single user (client) or a client network.

As per Wang et al each CCM processes the commands received from the clients, schedules the playback of the multiple video streams, manages the video file structure and controls the flow of video data to the DM (or DM's) to ensure real-time playback. Each DM is also a conventional computer equipped with a conventional SCSI controller card operating in a "target" mode. In addition to having a SCSI controller, the DM's are each equipped with one or more processing modules for processing the video stream prior to delivery to the client. In one embodiment, the processing modules are video decoders, each dedicated to decompressing a video data stream. In this embodiment as taught by Wang et al the processing modules are conventional network interface cards for formatting the video stream and delivering the video stream to a client over a network such as an ethernet, Asynchronous Transfer Mode (ATM), or Public Switched Telephone Network (PSTN) network and the like. Additionally, each DM has local memory used as a video buffer for storing video data prior to processing on the DM. Each SM is a high capacity storage medium adapted to store digital information such as video data and is accessed by the CCM module using standard SCSI protocol. Each SM, for example is a hard disk, or CD-ROM drive or a bank of hard disks or a bank of CD-ROMS or another type of high capacity storage medium.

Further in accordance with Wang et al, the CCM manages the file system using a hybrid file management scheme to obtain increased performance in data

access and to improve memory utilization. The hybrid file management scheme employs both the file management system that is included in the conventional operating system running on the CCM as well as customized file management software that bypasses the conventional file manager in order to directly control and access raw video data stored on the storage devices. This hybrid scheme optimizes access time with respect to video data yet utilizes the file management services of the operating system to manage the control information associated with the raw video data as well as the video storage maps. See column 3, lines 35 – 67 of Wang et al.

U.S. Patent Number 6,253,271 (Ram et al) discloses, in FIG. 1 thereof, a computer system having a plurality of loosely-coupled processors that collectively provide a high-performance file server is illustrated. One or more client computers 90 are connected over a network 100 to one or more network processors (NP)'s 110 and 112. Each of NPs 110 and 112 has one or more network interlace cards (NIC)'s 112 which are connected to the network 100. In the illustrated embodiment, the NIC's 112 are connected into a peripheral component interconnect (PCI) bridge 114. The PCI bridge 114 in turn is connected to a central processing unit (CPU) 116 which supplies processing capability for the NP 110. The CPU 116 receives data and instructions from a random access memory (RAM) 118. The RAM 118 preferably supports a read cache which buffers network request data in case the client 90 requests previously retrieved data. To increase the performance of the system, the system of FIG. 1 leverages a unified memory image capability of the system, which means that all processors can access the same memory space, to provide caches having segments which are dynamically allocatable to different NPs.

The dynamic allocation process reduces the need to move or shift data around the system of FIG 1 by having a plurality of file storage processors (FSP)'s which monitor the location of cached files such that when an incoming request from one NP results in a hit in the read cache of a second NP, the responding FSP can simply request the second NP to respond. In this manner the read cache of the individual NPs is global, resulting in additional efficiencies and performance gain as disk accesses are minimized.

As per Ram et al the CPU 116 is also shown connected to a second bridge 122, a PCI bridge, which in turn is connected to an interconnect bus 120, such as a scalable coherent interface (SCI), via a card 124. The SCI interconnect bus 120 may be deployed in a number of topologies, including a ring configuration where sub-systems are connected as a ring which does not support hot-pluggability. Alternatively, the SCI interconnect 120 may be a multi-ported switch where each sub-system is on its own SCI ring and therefore can be hot-plugged. Additional port switches can be used to improve the system bandwidth. The standard SCI interconnect uses five meter point-to-point cabling with two fifty-pin high density Small Computer System Interface (SCSI) style connectors. The network processors 110 and 112 provide all protocol processings between a network layer data format and an internal file server format for communicating client requests to other NPs and FSP's in the system.

In Ram et al according to the illustrated embodiment, data is supplied to clients 90 from one or more file storage processors (FSP)'s 150 and 160 which are connected to the SCI interconnect bus 120, The FSP 150 connects to the SCI interconnect bus 120 using an SCI interface 130. The SCI interface 130 is

connected to a buffer bridge 132 and a PCI bridge 134. The PCI bridge 134 in turn is connected to a CPU 136, which handles host processing operations as well as file processing operations. The CPU 136 is connected to a RAM 138 which supports a metadata cache as well as a write cache to increase file storage access requests. The metadata cache in the RAM 138 contains file management information, including a directory name look-up table, among others. The directory name look-up table is used to speed up directory search operations, as UFS directories are flat and must be searched sequentially. Further, the directory name look-up table maintains hits and misses for short file names. In the directory name look-up table, data structures are kept in a least recently used (LRU) order and maintained as a hashed table. The CPU 136 is also connected to a second PCI bridge 140 which in turn is connected to one or more disk controllers 142 and 144. The disk controllers 142 and 144 in turn drive a plurality of data storage devices 146 and 148, The buffer bridge 132 is also connected to the PCI bridge 140 to provide a path that enables network processors 110 and 112 that are connected to the SCI interconnect bus 120 to directly communicate with data storage devices 146-148 via disk controllers 142-144.

As taught in Ram et al a short-cut path is provided through which the client 90 can receive data from the combination of disk controllers 142-144 and data storage devices 146-148 via the buffer bridge 132. As the local CPU 136 and the RAM 138 of the file storage processor 150 are minimally involved in the disk operation, response times to data storage requests from the client 90 are reduced. Further, the contention for local FSP buses is reduced. Additionally, the CPU 136 as well as the RAM 138 of the file storage processor 150 are available for handling other tasks

required of the file storage processor 150. The off-loading of tasks from the CPU 136 and the RAM 138 ultimately results in a more responsive server system. See column 3, line 10 to column 4, line 31 and Fig. 1.

U.S. Patent Number 6,513,097 (Beardsley et al) discloses a storage controller 2 in Fig. 1 which interfaces between host computers or devices (not shown) and DASDs 46, 48. The DASDs may be organized in a redundant array of independent disks, i.e., a RAID array. In preferred embodiments, the storage controller 2 is divided into two clusters, cluster 0 and cluster 1. Cluster 0 consists of host adapters 4, 6, a nonvolatile storage unit (NVS) 8, a cache 10, a processor 12, a device adapter bus 14, device adapters 16, 18, 20, 22. Cluster 1 consists of host adapters 24, 26, an NVS 28, a cache 30, a processor 32, a device adapter bus 34, and device adapters 36, 38, 40, 42. A host adapter bridge 44 interfaces the components of cluster 0 with cluster 1. The host adapters 4, 6, 24, 26 are connected to the host adapter bridge 44.

In Beardsley et al according to the preferred embodiments, the bridge 44 is a dual master bus which may be controlled by one of the processors 12, 32 or one of the host adapters 4, 6, 24, 26. In further embodiments, the host adapter bridge 44 may include bridge technology to allow the bus to operate at its own clock speed and provide a buffer to buffer data transferred across the bridge 44. The bridge 44 interconnects the host adapters 4, 6, 24, 26 with the processors 12, 32. In preferred embodiments the processors 12, 32 are symmetrical multi-processors. Column 3, lines 35-65, column 4, lines 1-25.

b. Distinctions Between the References and the Claims

The present invention as recited in the claims is not taught or suggested by Wang et al, Ram et al or Beardsley et al whether taken individually or in combination

with each other or in combination with any of the other references now of record. The present invention as recited in the claims is directed to a storage system that is capable of being connected to a plurality of different types of networks, and a method of controlling activation of the storage system. The storage system of the present invention as recited in the claims includes, for example, a plurality of storage devices in which information is stored, a storage device control section that controls storage of information in the storage devices, and a connection unit connected to the storage device control section.

The storage system according to the present invention further includes a first communication control section having a first processor that is connected on a first network external to the storage system, that converts information of a first form, which is received over the first external network, into information of a second form, and that issues a request for access to the storage devices, and a second processor that accesses the storage devices via the connection unit and storage device control section, in response to the access request issued from the first processor, and that controls activation of the first processor.

The above described features of the present invention are not taught or suggested by Wang et al, Ram et al or Beardsley et al whether taken individually or in combination with each other or in combination with any of the other references now of record.

c. Remaining References

U.S. Patent No. 5,285,528 (Hart) discloses data structures and algorithms for managing lock states of addressable element ranges.

U.S. Patent No. 5,504,873 (Martain et al) discloses a mass data storage and

retrieval system.

U.S. Patent No. 5,548,724 (Akizawa et al) discloses a file server system and file access control method.

U.S. Patent No. 5,659,718 (Osman et al) discloses a high performance synchronous bus and bus interface device for interconnecting numerous devices without using dedicated high current drivers at each device.

U.S. Patent No. 5,671,377 (Bleidt et al) discloses a system for supplying streams of data to multiple users by distributing a data stream to multiple processors and enabling each user to manipulate supplied data stream.

U.S. Patent No. 5,710,881 (Gupta et al) discloses a data merging method and apparatus for shared memory multiprocessing computer systems.

U.S. Patent No. 5,774,731 (Higuchi et al) discloses an exclusive control method with each node controlling issue of an exclusive use request to a shared resource, a computer system therefore and a computer system with a circuit for detecting writing of an event flag into a shared main storage.

U.S. Patent No. 5,832,222 (Dziadosz et al) discloses an apparatus for providing a single image of an I/O subsystem in a geographically dispersed computer system.

U.S. Patent No. 6,006,342 (Beardsley et al) discloses a failover and failback system for a direct access storage device.

U.S. Patent No. 6,078,990 (Frazier) discloses a volume set configuration using a single operational view.

U.S. Patent No. 6,105,122 (Muller et al) discloses an I/O protocol for highly configurable multi-node processing system.

U.S. Patent No. 6,173,374 (Heil et al) discloses a system and method for peer-

to-peer accelerated I/O shipping between host bus adapters in clustered computer network.

U.S. Patent No. 6,330,604 (Higuchi et al) discloses an exclusive control method with each node controlling issue of an exclusive use request to a shared resource, a computer system therefore and a computer system with a circuit for detecting writing of an event flag into a shared main storage.

U.S. Patent No. 6,421,711 (Blumenau et al) discloses virtual ports for data transferring of a data storage system.

U.S. Patent No. 6,438,586 (Hass et al) discloses a file transfer utility which employs an intermediate data storage system.

U.S. Patent No. 6,502,136 (Higuchi et al) discloses an exclusive control method with each node controlling issue of an exclusive use request to a shared resource, a computer system therefore and a computer system with a circuit for detecting writing of an event flag into a shared main memory.

6. Fee (37 C.F.R. 1.17(i))

The fee required by 37 C.F.R. § 1.17(i) is to be paid by:

[X] the Credit Card Payment Form (attached) for $130.00.

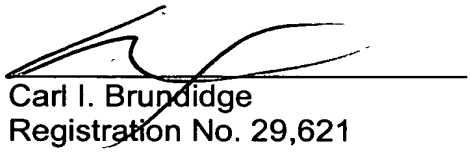
[ ] charging Account _____ the sum of $130.00.

A duplicate of this petition is attached.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (501.43126X00).

Respectfully submitted,

Antonelli, Terry, Stout & Kraus, LLP



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Enclosures